10-Bit High Speed Multiplying D/A Converter (Universal Digital Logic Interface)

DAC10*

FEATURES
Fast Settling: 85 ns
Low Full-Scale Drift: 10 ppm/°C
Nonlinearity to 0.05% Max Over Temperature Range
Complementary Current Outputs: 0 mA to 4 mA
Wide Range Multiplying Capability: 1 MHz Bandwidth
Wide Power Supply Range: +5, –7.5 Min to ±18 V Max
Direct Interface to TTL, CMOS, ECL, PMOS, NMOS
Availability in Die Form

GENERAL DESCRIPTION

The DAC10 series of 10-bit monolithic multiplying digital-to-analog converters provide high speed performance and full-scale accuracy.

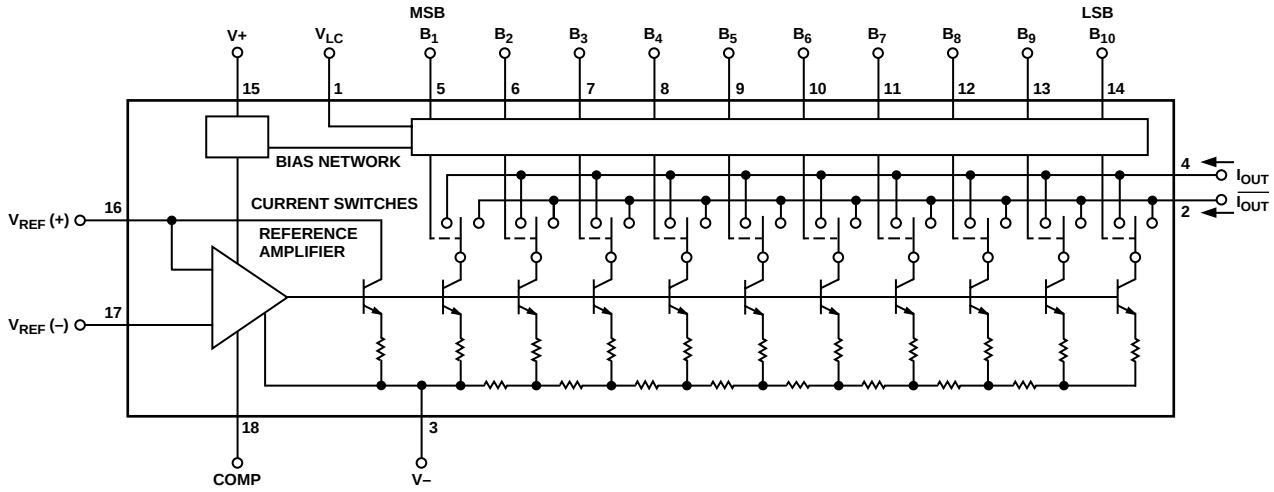
Advanced circuit design achieves 85 ns settling times with very low "glitch" energy and low power consumption. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

All DAC10 series models guarantee full 10-bit monotonicity, and nonlinearities as tight as +0.05% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±18 V power supply range, with 85 mW power consumption attainable at lower supplies.

A highly stable, unique trim method is used, which selectively shorts Zener diodes, to provide 1/2 LSB full-scale accuracy without the need for laser trimming.

Single-chip reliability, coupled with low cost and outstanding flexibility, make the DAC10 device an ideal building block for A/D converters, Data Acquisition systems, CRT displays, programmable test equipment and other applications where low power consumption, input/output versatility and long-term stability are required.

SIMPLIFIED SCHEMATIC



*Protected by Patent Nos. 4,055,770, 4,056,740 and 4,092,639.

REV. D

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DAC10–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ V_S = ±15 V; I_{REF} = 2 mA; 0°C ≤ T_A ≤ +70°C for DAC10F and G, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter	Symbol	Conditions	DAC10F Min	DAC10F Typ	DAC10F Max	DAC10G Min	DAC10G Typ	DAC10G Max	Units
MONOTONICITY			10			10			Bits
NONLINEARITY	NL			0.3	0.5		0.6	1	LSB
DIFFERENTIAL NONLINEARITY	DNL			0.3	1		0.7		LSB
SETTLING TIME	t_S	All Bits Switched ON or OFF Settle to 0.05% of FS (See Note)		85	135		85	150	ns
OUTPUT CAPACITANCE	C_O			18			18		pF
PROPAGATION DELAY	t_{PLH} t_{PHL}	All Bits Switched R_L = 5 kΩ R_L = 0 kΩ		50 50			50 50		ns ns
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	Full-Scale Current Change <1 LSB		–5.5 +10			–5.5 +10		V V
GAIN TEMPCO	TCI_{FS}	(See Note)		±10	±25		±10	±50	ppm/°C
FULL-SCALE SYMMETRY	I_{FSS}	I_{FR}–$\overline{I_{FR}}$		0.1	4		0.1	4	µA
ZERO-SCALE CURRENT	I_{ZS}			0.01	0.5		0.01	0.5	µA
FULL-SCALE CURRENT	I_{FR}	(See Note)	3.960	3.996	4.032	3.920	3.996	4.072	mA
REFERENCE INPUT SLEW RATE	DI/dt			6			6		mA/µs
REFERENCE BIAS CURRENT	I_B			–1	–3		–1	–3	µA
POWER SUPPLY SENSITIVITY	$PPS/_{FS}$+ $PPS/_{FS}$–	4.5 V ≤ V+ ≤ –18 V –18 V ≤ V– ≤ –10 V		0.001 0.0012	0.01 0.01		0.001 0.0012	0.01 0.01	$\%\Delta I_{FS}/\%\Delta V$ $\%\Delta I_{FS}/\%\Delta V$
POWER SUPPLY CURRENT	I+ I– I+ I–	V_S = ±15 V; I_{REF} = 2 mA V_S = +5 V; –7.5 V; I_{REF} = 1 mA 		2.3 –9 1.8 –5.9	4 –15 4 –9		2.3 –9 1.8 –5.9	4 –15 4 –9	mA mA mA mA
POWER DISSIPATION	P_D P_D	V_S = ±15 V; I_{REF} = 2 mA V_S = +5 V; –7.5 V; I_{REF} = 1 mA		231 85	285 88		231 85	285 88	mW mW
LOGIC INPUT LEVELS	V_{IL} V_{IH}	V_{LC} = 0 V_{LC} = 0	2		0.8	2		0.8	V V
LOGIC INPUT CURRENTS	I_{IL} I_{IH}	V_{LC} = 0; V_{IN} = 0.8 V V_{IN} = 2.0 V	–10	–5 0.001	 10	–10	–5 0.001	 10	µA µA

ELECTRICAL CHARACTERISTICS

(@ V_S = ±15 V; I_{REF} = 2 mA; T_A = +25°C, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter	Symbol	Conditions	DAC10F Min	DAC10F Typ	DAC10F Max	DAC10G Min	DAC10G Typ	DAC10G Max	Units
MONOTONICITY			10			10			Bits
NONLINEARITY	NL			0.3	0.5		0.6	1	LSB
DIFFERENTIAL NONLINEARITY	DNL			0.3	1		0.7		LSB
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	Full-Scale Current Change, <1 LSB	–5	–6/+18	+10	–5	–6/+15	+10	V
FULL-SCALE CURRENT	I_{FS}	V_{REF} = 10.000 V, R14 = R15 = 5.000 kΩ	3.978	3.996	4.014	3.956	3.996	4.036	mA
FULL-SCALE SYMMETRY	I_{FSS}	I_{FR}–$\overline{I_{FR}}$		0.1	4		0.1	0.4	µA
ZERO-SCALE CURRENT	I_{ZS}			0.01	0.5		0.01	0.5	µA

NOTE: Guaranteed by design.

WAFER TEST LIMITS

(@ V_S = ±15 V, I_{REF} = 2 mA, T_A = +25°C, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$).

Parameter	Symbol	Conditions	DAC10N Limit	Units
RESOLUTION			10	Bits min
MONOTONICITY			10	Bits min
NONLINEARITY	NL		±0.5	LSB max
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	True 1 LSB	+10 –5	V max V min
OUTPUT CURRENT RANGE		I_{FS} ±3.996 mA	±18	μA max
ZERO-SCALE CURRENT	I_{ZS}	All Bits OFF	0.5	μA max
LOGIC INPUT "1"	V_{IH}	I_{IN} = 100 nA	2	V min
LOGIC INPUT "0"	V_{IL}	V_{LC} @ Ground I_{IN} = –100 μA	0.8	V max
POSITIVE SUPPLY CURRENT	I+	V+ = 15 V	4	mA max
NEGATIVE SUPPLY CURRENT	I–	V+ = –15 V	–15	mA max

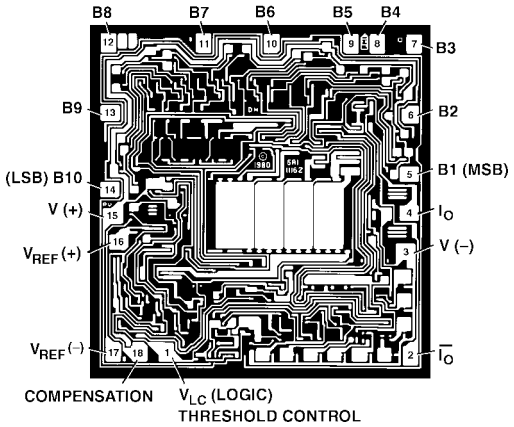
NOTE: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard produce dice.

TYPICAL ELECTRICAL CHARACTERISTICS

(@ V_S = ±15 V, I_{REF} = 2 mA, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$).

Parameter	Symbol	Conditions	DAC10F Typ	Units
SETTLING TIME	t_S	To ±1/2 LSB When Output Is Switched from 0 to FS	85	ns
GAIN TEMPERATURE COEFFICIENT (TC)		V_{REF} Tempco Excluded	±10	ppm FS/°C
OUTPUT CAPACITANCE			18	pF
OUTPUT RESISTANCE			10	MΩ

DICE CHARACTERISTICS



DIE SIZE 0.091 × 0.087 inch, 7,917 sq. mils
(2.311 × 2.210 mm, 5.107 sq. mm)

ABSOLUTE MAXIMUM RATINGS[1]

Operating Temperature
DAC10FX, GX, GS, GP . . . . . 0°C to +70°C
Junction Temperature (T_J) . . . . . –65°C to +150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C
V+ Supply to V– Supply . . . . . 36 V
Logic Inputs . . . . . V– to V– plus 36 V
V_{LC} . . . . . V– to V+
Analog Current Outputs . . . . . +18 V to –18 V
Reference Inputs (V_{16} to V_{17}) . . . . . V– to V+
Reference Input Differential Voltage (V_{16} to V_{17}) . . . . ±18 V
Reference Input Current (I_{16}) . . . . . 2.5 mA

Package Type	θ_{JA}[2]	θ_{JC}	Units
18-Lead Hermetic DIP (X)	48	15	°C/W
18-Lead SOIC (S)	89	28	°C/W
18-Lead Plastic DIP (P)	74	33	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for Cerdip packages.

ORDERING GUIDE

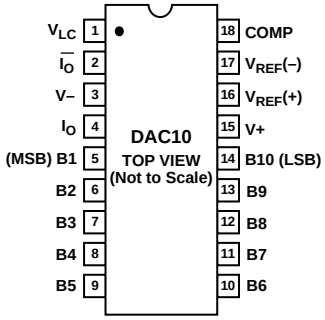
Model	INL (LSB)	Temperature Range	Package Description	Package Options
DAC10FX	0.5	0°C to +70°C	Cerdip	Q-18
DAC10GX	1	0°C to +70°C	Cerdip	Q-18
DAC10GS	1	0°C to +70°C	SOIC	R-18
DAC10GP	1	0°C to +70°C	Plastic DIP	N-18

PIN CONNECTIONS

18-Lead Hermetic DIP

18-Lead Plastic DIP

18-Lead SOIC



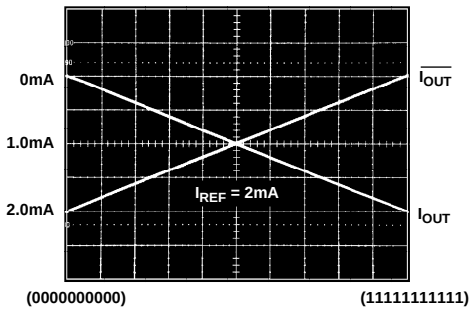


Figure 1. True and Complementary Output Operations

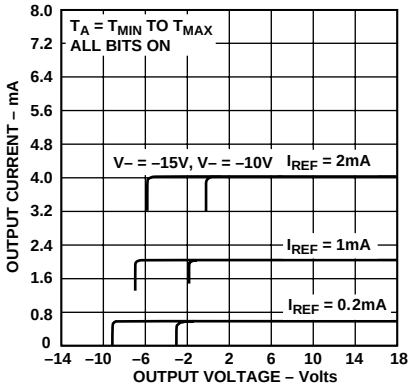


Figure 2. Output Current vs. Output Voltage (Output Voltage Compliance)

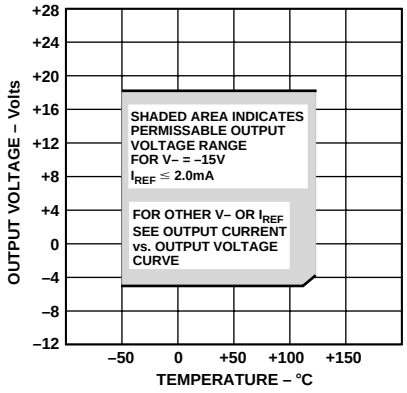


Figure 3. Output Voltage Compliance vs. Temperature

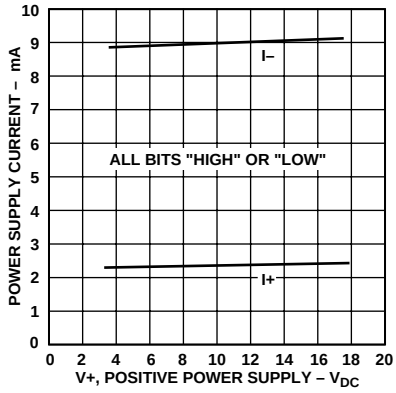


Figure 4. Power Supply Current vs. V+

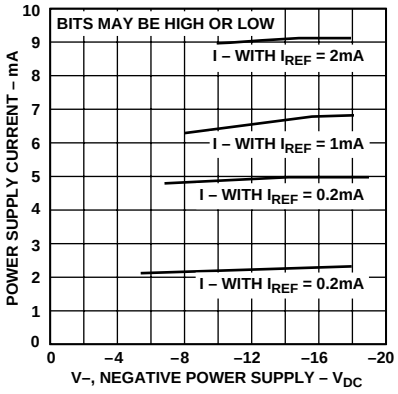


Figure 5. Power Supply Current vs. V–

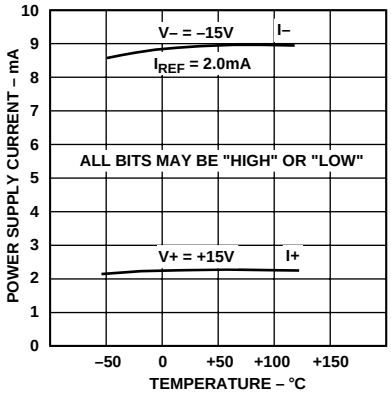


Figure 6. Power Supply Current vs. Temperature

BASIC CONNECTIONS

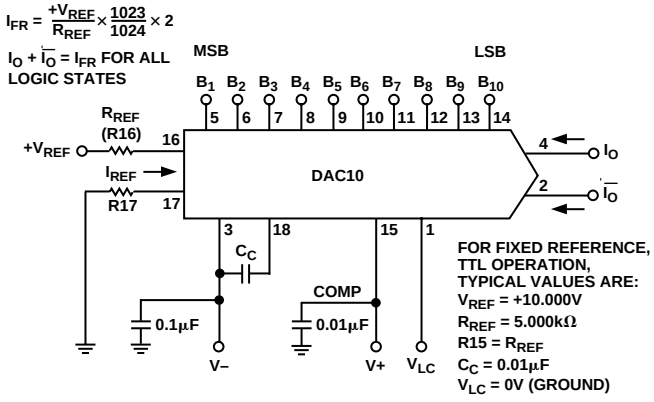


Figure 7. Basic Positive Reference Operation

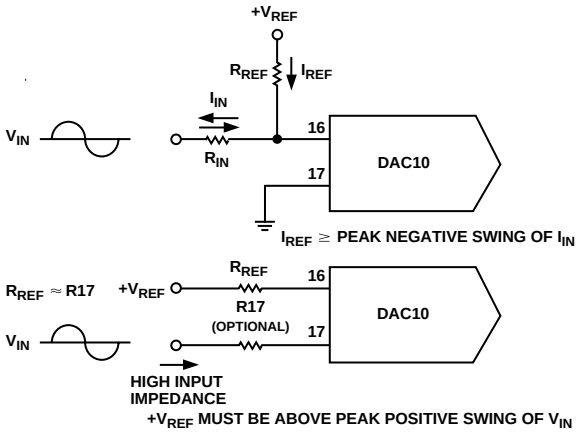


Figure 8. Accommodating Bipolar References

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection.

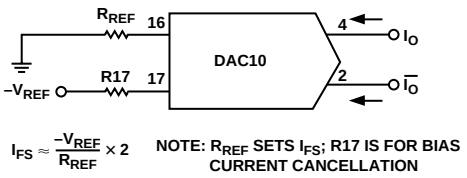


Figure 9. Basic Negative Reference Operation

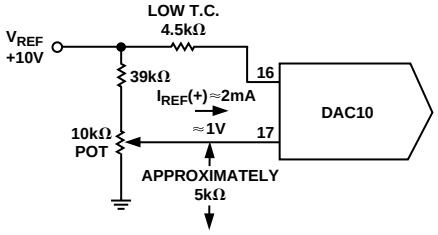
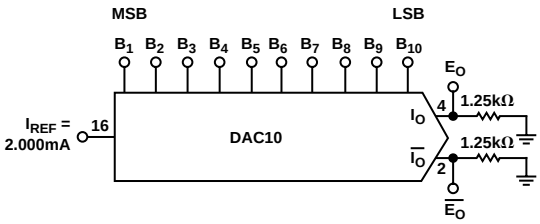
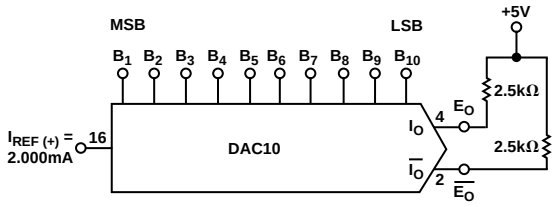


Figure 10. Recommended Full-Scale Adjustment Circuit



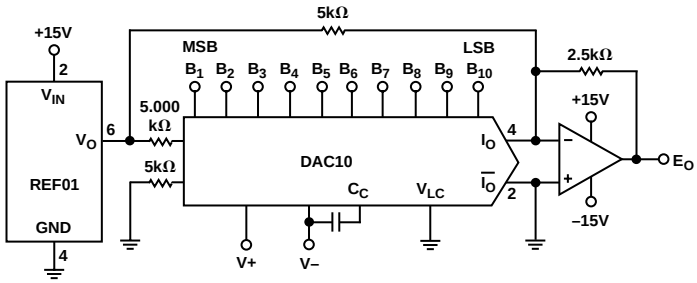
	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	I_OmA	$\overline{I_O mA}$	E_O	$\overline{E_O}$
FULL RANGE	1	1	1	1	1	1	1	1	1	1	3.996	0.000	–4.995	–0.000
HALF-SCALE +LSB	1	0	0	0	0	0	0	0	0	1	2.004	1.992	–2.505	–2.490
HALF-SCALE	1	0	0	0	0	0	0	0	0	0	2.000	1.996	–2.500	–2.495
HALF-SCALE –LSB	0	1	1	1	1	1	1	1	1	1	1.996	2.000	–2.495	–2.500
HALF-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	0.004	3.992	–0.005	–4.990
ZERO SCALE +LSB	0	0	0	0	0	0	0	0	0	0	0.000	3.996	0.000	–4.995

Figure 11. Basic Unipolar Negative Operation



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	E_O	$\overline{E_O}$
POSITIVE FULL RANGE	1	1	1	1	1	1	1	1	1	1	–4.990	+5.000
POSITIVE FULL RANGE –LSB	1	1	1	1	1	1	1	1	1	0	–4.980	+4.990
ZERO-SCALE +LSB	1	0	0	0	0	0	0	0	0	1	–0.010	+0.020
ZERO-SCALE	1	0	0	0	0	0	0	0	0	0	0.000	+0.010
ZERO-SCALE –LSB	1	1	1	1	1	1	1	1	1	1	+0.010	0.000
NEGATIVE FULL-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	+4.990	–4.980
NEGATIVE FULL-SCALE	0	0	0	0	0	0	0	0	0	0	+5.000	–4.990

Figure 12. Basic Bipolar Output Operation



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	E_O
POSITIVE FULL RANGE	1	1	1	1	1	1	1	1	1	1	+4.990
ZERO-SCALE	1	0	0	0	0	0	0	0	0	0	0.00
NEGATIVE FULL-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	–4.990
NEGATIVE FULL-SCALE	0	0	0	0	0	0	0	0	0	0	–5.000

Figure 13. Offset Binary Operation

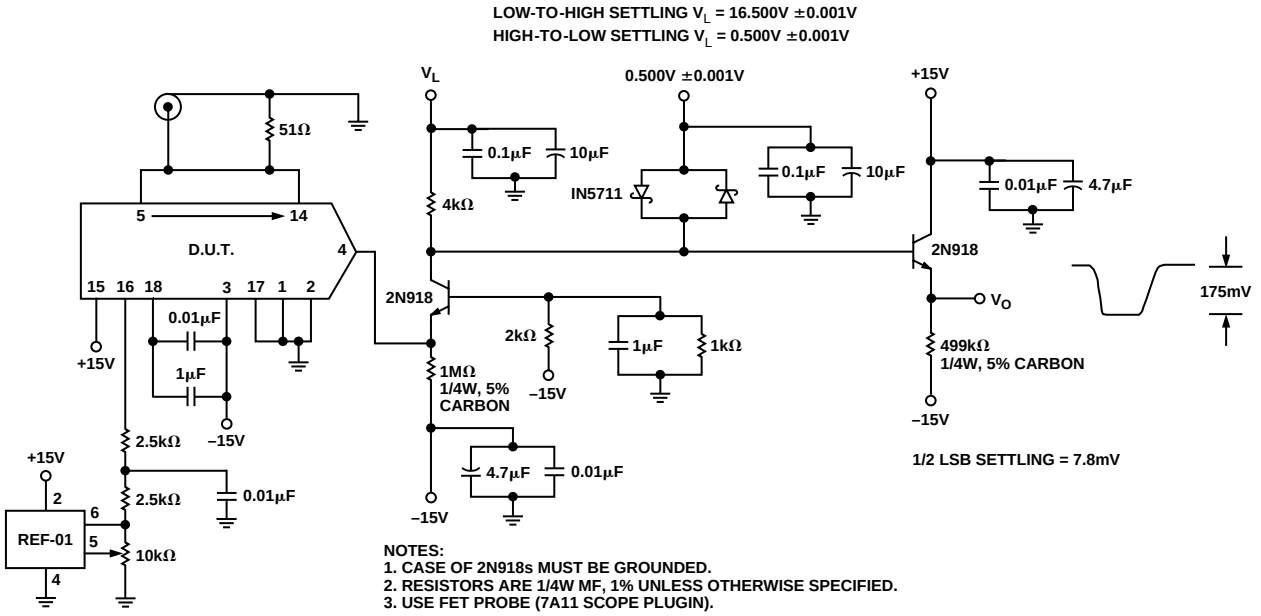


Figure 14. Settling Time Measurement

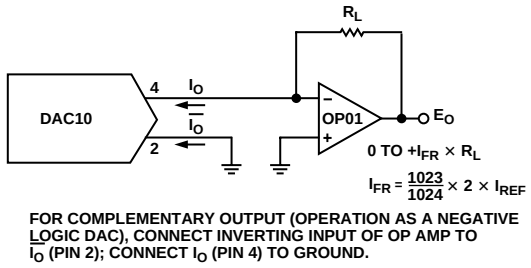


Figure 15. Positive Low Impedance Output Operation

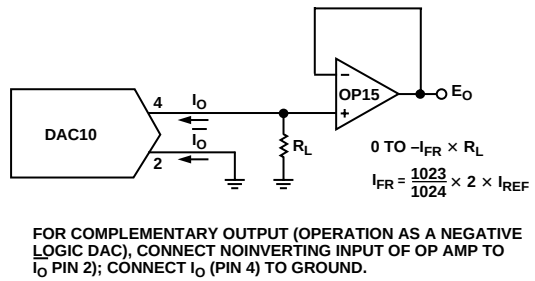


Figure 16. Negative Low Impedance Output Operation

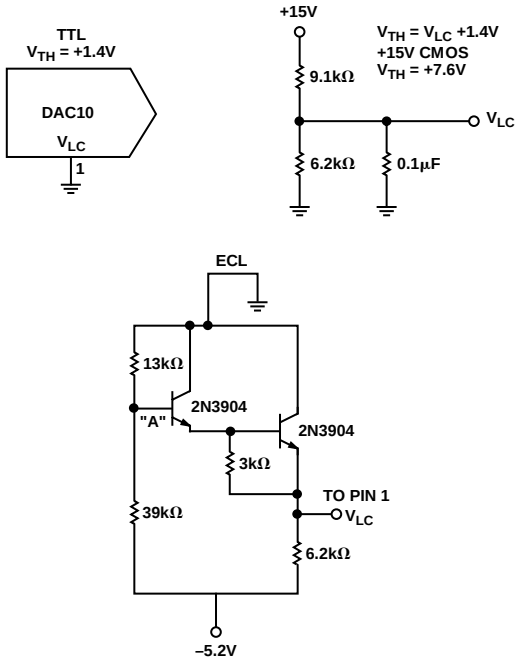


Figure 17. Interfacing with Various Logic Families

APPLICATIONS

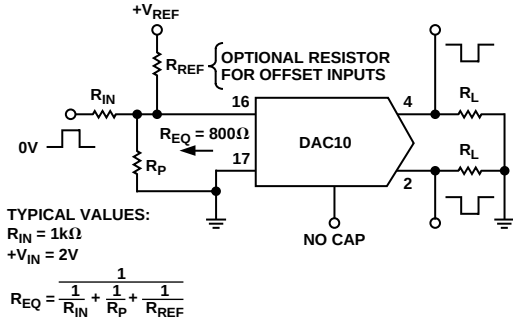


Figure 18. Pulsed Reference Operation

Reference Amplifier Setup

The DAC10 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to 2 mA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{1023}{1024} \times 2 \times I_{REF}$$

where I_{REF} equals current flowing into Pin 16.

In positive reference applications, an external positive reference voltage forces current through R16 into the V_{REF} (+) terminal (Pin 16) of the reference amplifier. Alternatively, a negative reference may be applied to V_{REF} (–) at Pin 17; reference current flows from ground through R16 into V(+) as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 17. R17 (nominally equal to R16) is used to cancel bias current errors; R17 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or Pin 17. The negative common-mode range of the reference amplifier is given by: V_{CM}– = V– plus ($I_{REF} \times 2$ kΩ) plus 2 V. The positive common-mode range is V+ less 1.8 V.

When a dc reference is used, a reference bypass capacitor is recommended. A 5 V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R16 should be split into two resistors with the junction bypassed to ground with a 0.1 μF capacitor.

For most applications, the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R16, or by using a potentiometer for R16. An improved method of full-scale trimming that eliminates potentiometer TC effect is shown in the Recommended Full-Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from Pin 18 to V–. For fixed reference operation, a 0.01 μF capacitor is recommended. For variable reference applications, see section entitled Reference Amplifier Compensation for Multiplying Applications.

Multiplying Operation

The DAC10 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4 mA to 4 μA. Monotonic operation is maintained over a typical range of I_{REF} from 100 μA to 2 mA.

Reference Amplifier Compensation for Multiplying Applications

AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 18 to V–. The value of this capacitor depends on the impedance presented to Pin 16 for R16 values of 1.0 kΩ, 2.5 kΩ and 5.0 kΩ, minimum values of C_C are 15 pF, 37 pF and 75 pF. Larger values of R16 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R16 enabling small C_C values should be used. If Pin 16 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated, which will decrease overall bandwidth and slew rate. For R16 = 1 kΩ and C_C = 15 pF, the reference amplifier slews at 4 mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 2 mA in 500 ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 mA to 2 mA) occurs in 120 ns when the equivalent impedance at Pin 16 is 200 Ω and C_C = 0. This yields a reference slew rate of 16 mA/μs, which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC10 design incorporates a unique logic input circuit that enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2 μA logic input current and completely adjustable logic threshold voltage. For V– = –15 V, the logic inputs may swing between –5 and +18 V. This enables direct interface with +15 V CMOS logic, even when the DAC10 is powered from a +5 V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V– plus ($I_{REF} \times$ 2 kΩ) plus 3 V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control Pin (Pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 V above V_{LC}. For TTL interface, simply ground Pin 1. When interfacing ECL, an I_{REF} = 1 mA is recommended. For interfacing other logic families, see Figure 17. For general setup of the logic control circuit, it should be noted that Pin 1 will sink 1.1 mA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a 1 kΩ divider, for example, it should be bypassed to ground by a 0.01 μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at Pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at Pin 4 and turned on at Pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required, it must still be connected to ground or to a point capable of sourcing I_{FS}. DO NOT LEAVE AN UNUSED OUTPUT PIN OPEN.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36 V above V– and is independent of the positive supply. Negative compliance is +10 V above V–.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC10 operates over a wide range of power supply voltages from a total supply of 9 V to 36 V. When operating with V– supplies of –10 V or less, $I_{REF} \leq 1$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range and negative logic threshold range; consult the various figures for guidance. For example, operation at –9 V with I_{REF} = 2 mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8 V total must be applied to ensure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC10 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to ensure that logic swings, etc., remain within acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC10 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically +10 ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor, R14, should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC10 decrease approximately 10% at –55°C; an increase of about 15% is typical at +125°C.

SETTLING TIME

The DAC10 is capable of extremely fast settling times; typically 85 ns at I_{REF} = 2 mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35 ns for each of the 10 bits. Settling time to within 1/2 LSB of the LSB is therefore 35 ns, with each progressively larger bit taking successively longer. The MSB settles in 85 ns, thus determining the overall settling time of 130 ns. Settling to 8-bit accuracy requires about 60 ns to 78 ns. The output capacitance of the DAC10, including the package, is approximately 18 pF; therefore, the output RC time constant dominates settling time if $R_L > 500\ \Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1 mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±2 μA; therefore, a 4 kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of schematic titled "Settling Time Measurement" uses a cascode design to permit driving a 4 kΩ load with less than 5 pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1 mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 0111111111 to 1000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

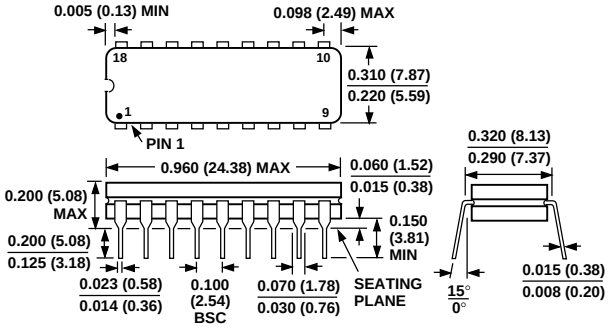
DAC10 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output with a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1 μF capacitors at the supply pins provide full transient protection.

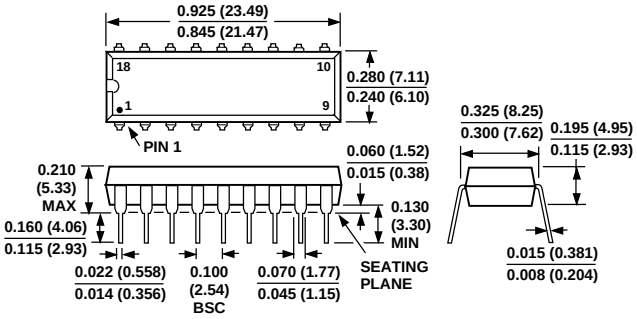
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

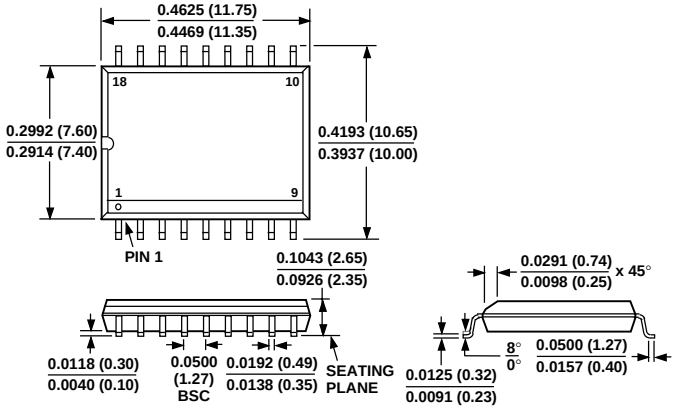
18-Lead Cerdip
(Q-18)



18-Lead Plastic DIP
(N-18)



18-Lead Wide Body SOL
(R-18)



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